ERROR CORRECTION DEVICE

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to error correction, and more specifically, to an error correction device used for optical disks having a data structure composed of a main data unit and a parity unit.

(2) Description of the Prior Art

In recent years, DVDs (digital versatile discs) and CD-ROMs (compact disc-read-only memories) for recording digital data at high densities have come to be widely used. The digital data, which are recorded or read by a laser, are very small in size. No matter how carefully these media may be fabricated or handled, it is difficult to prevent them from getting fingerprints or blemishes on their surface.

Hence, the use of error correcting technology is essential. However, in such a case where 1-bit parity is merely appended to every 7-bit main data, if an error arises, its presence is known but its location and the original data remain unknown. Moreover, if two errors arise, their occurrence itself is unknown. To solve this problem, as shown in Figures 1 and 2, error correction is performed by providing data with parity having a complicated structure in the vertical and the horizontal direction. According to this system, even if several errors arise, they will be found in real time and corrected.

There have been various techniques developed as methods for appending parity, one of them being RS code correction which comes down

error correction to a question of solving a numerical formula. Since RS code correction is a known art shown in *FUGO RIRON NYUMON* or *Introduction to the Theory of Codes* written by Iwatare and published by Shoseido, *JISSEN AYAMARI TEISEI GIJUTU*, or *A Hands-on Technique of Error Correction* published by TRICEPTS, and the like, its description will be omitted.

In optical disks such as DVDs and CD-ROMs, error correction of data is performed in compliance with individual data formats.

The following is a description of error correction for a DVD. The data format in one sector is shown in Figure 1, and the data format in one block including error correcting codes (ECCs) is shown in Figure 2. As shown in Figure 1, one sector includes a header, main data, and an error detecting code (EDC). The block including the ECCs shown in Figure 2 contains the sector shown in Figure 1, and has product codes with inner code parity for horizontal error correction and outer code parity for vertical error correction. (In the present specification, as a rule, the sector shown in Figure 1 + the inner code parity on the right side in Figure 2 is referred to as a sector).

In an error correction device for DVDs, it is general that demodulated data are temporarily written in the buffer memory and read later in order to execute error correction for the data in the buffer memory because error correction in real time takes much time, considering it is done by an electronic device, and has to be repeated until no error is left. In this case, there are horizontal error correction with inner code parity and vertical error correction with outer code parity.

In horizontal error correction for consecutive main data such as image data, syndrome calculation is performed every code word (string) (consisting of 172-byte data and 10-byte inner code parity) to detect an error-containing code, and error correction is performed by calculating the position and value of the error, based on the data of the detected code. In vertical error correction, syndrome calculation is performed every code word (consisting of 192-byte data and 16-byte outer code parity) to detect an error-containing code, and the position and value of the error are calculated, based on the data of the detected code. Following error correction repeated for a predetermined number of times in the horizontal direction first and then in the vertical direction, error detection is performed in order to check to see that no error remains in the data (or that the error correction is successfully done) by using each EDC. If no error is detected, this means that the error correction is complete.

Then, data in the buffer memory whose error has been corrected are transmitted downstream, and data in the next sector obtained from upstream are written in the buffer memory.

A prior art error correction device is shown in Figure 3. This device comprises a system control unit 1 which controls the entire system, a DMA control unit 2 which controls DMA (direct memory access) transfer described below between buffer memory and each unit, a bus control unit 3, a buffer memory 4 which stores demodulated data, a syndrome calculator 5 for generating syndrome that is an equation to be solved for error correction, an error corrector 6 which performs error correction by calculating the position and value of an error, based on the syndrome